

[illegible]

Figure 1 is a schematic diagram of the proposed 128-bit cryptographic architecture. It shows a 128-bit input being split into two 64-bit paths. The top path goes through a 64-bit S-box and a 64-bit permutation block. The bottom path goes through a 64-bit S-box and a 64-bit permutation block. The outputs of these two paths are then combined in a 128-bit permutation block. The final output is a 128-bit stream. The diagram also shows a 128-bit key stream being generated from a 128-bit key and a 128-bit counter. The key stream is then XORed with the input to produce the output.

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<p><b>PROJETO ELÉTRICO</b></p> <p>PLANTA BAIXA - DIAGRAMA UNIFILAR - QUADRO DE CARGAS - LEGENDA</p>			
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